Docket No.: 3672-0144P
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Michael O. THOMPSON, et al.

Application No.: 10/088,913 Confirmation No.: 8909

Filed: May 7, 2002 Art Unit: 2824

For: NON-VOLATILE PASSIVE MATRIX DEVICE AND METHOD FOR READOUT OF THE SAME Examiner: J. H. Hur

REQUEST FOR A PRE-APPEAL BRIEF CONFERENCE

MS AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

September 5, 2006

Sir:

INTRODUCTORY COMMENTS

Applicants respectfully request review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed concurrently with a Notice of Appeal.

The review is being requested for the reasons set forth on the attached five (5) sheets.

ARGUMENTS

Applicants respectfully submit that the Examiner has made the following clear errors:

(1) The Examiner is improperly alleging that amendments made (specifically the addition of the term "ohmic contact") to the claims add new matter and is improperly rejecting claims 1, 2 and 13 under 35 U.S.C. §112, first paragraph for failing to comply with the written description requirement with regards to the alleged new matter added in the claims.

(2) The Examiner is improperly interpreting the cited references used in rejecting the independent claims 1, 12 and 13 under 35 U.S.C. §103(a) in view of Kuroda (U.S. 5,487,029) and Clemons (U.S. 4,599,709).

The Term "Ohmic Contact" Is Not New Matter And Is Supported By the Original Disclosure

Claims 1, 12 and 13 were amended to include the recitation of "where each memory cell is at all time in ohmic contact with a word line and a bit line," in order to clarify the distinction between passive memories and active memories. The present invention is directed to passive matrix memories. Passive matrix memories have no switching elements (active regions). The word and bit lines form a continuous matrix where each crossing point creates a memory cell and can be individually accessed electrically which entails providing a voltage across the memory cell. Therefore each memory cell is in ohmic contact with a word and bit line in which a voltage differentially is applied at each memory cell. This is a fundamental understanding of passive matrix memories.

A definition of ohmic is taken from McGraw-Hill Dictionary of Scientific and Technical Terms, Fifth Edition, page 1383 by Applicants. The definition states "a region where two materials are in contact, which has the property that the current flowing through it is proportional to the potential difference across it." Thus, ohmic contact refers to materials being in contact and a voltage potential across the materials. In passive matrix memories, this is accomplished at all times as the crossing points of word lines and bit lines. This understanding of passive matrix memories is explained at least at page 2, lines 2-9 of applicant's disclosure. Nonetheless, the understanding is inherent to passive matrix memories.

The Examiner in the Advisory Action dated August 22, 2006 states that the contacts could be non-ohmic and thus disagrees with applicants arguments. However, as stated above in passive matrix memories the contacts between word and bit lines are necessarily in ohmic contact in order to operate as a passive matrix and not require switching features necessary in active matrix memories.

Therefore, one of ordinary skill would understand this feature of passive matrix memories as a fundamental feature and therefore recognize applicant's had possession of this feature at the time of the invention. Further, applicants respectfully submit that no new matter is added. Accordingly, the objection and rejection of the added limitations is improper.

The Examiner Improperly Interprets Kuroda and Clemons Teachings

The applicant's claims recite a "passive matrix memory." Applicant's submit that the application of teaching of active matrix memories in Kuroda and Clemons is improper to teach features of a passive matrix memory. There is a fundamental difference between passive and active matrix memories. To further clarify this distinction applicant's amended the claims in the a Response filed on January 23, 2006, to recite that "each memory cell is at all times in ohmic contact with a word line and a bit line." This is a basic feature of passive matrix memories that cannot be taught by active or quasi-active matrix memories.

Applicants respectfully submit that each of references Clemons and Kuroda teach an active matrix memory. Applicants respectfully submit that the references do not teach a passive matrix addressable memory with segmented word lines. Applicants note that in a passive matrix there are no switching elements, for example, switching transistors. This is to say that all memory cells are permanently in ohmic contact with the electrodes, i.e. the word lines and bit lines of the memory. This is a problem pronounced in passive matrix addressable memories which is not as large of a problem in active memories. Thus, applicants embodiments are directed to addressing this problem by segmenting word lines addressing operations based on the segmentation. In an ordinary active matrix addressable memory each ferroelectric capacitor has a single switching element corresponding thereto. When randomly addressing a memory cell in an active matrix addressable ferroelectric memory, only the memory cells selected for addressing will be in ohmic contact with both electrodes and only during the addressing operation.

A solution to this problem, as disclosed in Kuroda is to employ memory units of the kind where one switching transistor is able to select more than one ferroelectric capacitor simultaneous. This of course means that one memory cell in the unit effected by the switching transistor is selected for an addressing operation and that the addressing operation can effect the other memory cells in the unit due to stray capacitances and voltage disturbs. For example, in Kuroda, a ferroelectric memory unit is comprised of eight memory cells in which one of the memory units is selected from the eight using the same switching transistor. In Kuroda, the memory is divided into separate memory blocks and as shown in Fig. 1, 16 memory blocks 00; 7, 7 thus forming a memory with 128 memory cells. The blocks are arranged to form columns of two blocks side by side and there is one sensing and writing means provided for each block in the module termed (WRCO) in Fig. 1. Each block contains 864 memory cells arranged in units of 8 sharing a common bit line and connectable via the switching transistor Q1 to a data line extending through and being common to both blocks in a column, i.e. Fig. 1, blocking 0, 0 and block 1, 0. Upon reading and writing a memory unit of each cell is selected via the selector to word line W1 and for a memory cell in the unit associated with the switching means Q1 can be addressed. The selection connects the bit line via the transistor Q1 with the data line D0 in this case one of the word lines W10....W17. A memory cell can be addressed for a read or write operation or either by the sensing means SA or write means WA, for which there is only provided one of each for each column of blocks.

Therefore, Kuroda is only able to address for read and write operations a single memory cell in a memory unit in one block at a time. However, in the case of having a memory with eight columns or blocks and one sense amplifier for each of the columns, the system can read in parallel eight memory cells, one from each block in a row. This, however, does not correspond to the word line segmentation of the present application.

Thus, Kuroda teaches a somewhat quasi-active matrix in which the memory cells are separated into groups or units and a single switching transistor is activated for that particular group or unit. Thus, only that group or unit is in ohmic contact during the addressing of that particular memory unit in that group or unit. In contrast, in the passive matrix addressable memory of the present invention all memory cells can be affected not just those in a particular group or unit because all memory cells are in continuous ohmic contact. Further, the memory block arrangement is the not the same as the claimed word line segmentation in a passive matrix memory as claimed.

Clemons is concerned with a static RAM memory which is an active type of memory. Clemons specifically states at column 4, lines 13-17 that "typical static memory cells employ two cross coupled field effect transistors" and that "each cell typically includes two access transistors." The Examiner has stated that Clemons has been provided to teach particular sensing means which can be combined in a passive matrix memory. Applicants respectfully submit that Clemons does not teach separating word lines into segments as claimed by applicants. In applicant's invention, the word lines are segmented because of the unique nature posed by the passive matrix memories as discussed above. By segmenting the word lines which allows for selection of all bit lines associated with those word lines is that each bit line is then associated with a specific sensing amplifier and read out. In Clemons, each bite block is separated based on the bit lines. Each bit line is accessed using one of transistors T200 through T203 as illustrated for bite block one. The addressing of the voltage on the bit lines to specific sense amplifiers is not based on segmentation of the word lines. This is further noticed in Fig. 3 in which each segmented bit lines, referred to as bite block one through eight, is provided and connected to the IO switches. In segmenting based on the word lines, as in embodiments of the present invention, all bit lines across the entire array associated with those word line segmentations can be sent simultaneously at the associated sensing means. As illustrated in Fig. 3, only the specific bit lines associated with a particular bite block can simultaneously be sensed. This is accomplished for each bite block.

Thus, applicants respectfully submit that the problem remains of Kuroda and Clemons being associated with active passive matrixes in which continuous ohmic contact between the word lines and bit lines is not taught. Further, Clemons does not teach or suggest word line segmentation, let alone to be implemented in a passive matrix memory.

Accordingly, applicants respectfully submit that the Examiner has improperly relied upon the teachings of Kuroda and Clemons to teach the claimed features of the passive matrix memory of the present invention.

Conclusion

In view of the foregoing, Applicant respectfully submits that the application is in condition for allowance. Favorable reconsideration and prompt allowance are earnestly solicited.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact Chad Billings (Reg. No. 48,917) at (703) 205-8001 **to schedule a Personal Interview**.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Dated: October 4, 2005

Respectfully submitted,

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